ABSTRACT:

The cascode circuit comprises a plurality of switching transistors (11) to be protected from high voltage and a plurality of cascode transistors (13) connected to the switching transistors (11). A test node (B') is arranged between each switching transistor (11) and its cascode transistor (13), and a test transistor (30.1-30.n) is allocated to each test node (B'), its gate being connected to the test node (B'). The sources of the test transistors (30.1-30.n) are connected to a first test point (31) and the drains of the test transistors (30.1-30.n) are connected to a second test point (32). A first voltage (U1) is applied to the first test point (31) and a second, slightly lower voltage (U2) is applied to the second test point (32). A current flow detected between the first (31) and the second (32) test point indicates that at least one of the cascode transistors (13) does not work correctly. Thus, the cascode circuit is testable. The high-density IC manufacturing process becomes applicable also for devices with a high number of high-voltage outputs. Internal potentials may be observed in a fast parallel way.

Figures 4 and 9